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TITLE

Method of checking overlap accuracy of patterns on four stacked semiconductor layers

Field of the Invention

The present invention relates to a method of checking overlap accuracy of patterns transferred on four stacked semiconductor layers, and more particularly to forming checking patterns on four stacked semiconductor layers and measuring overlap errors thereof by the method.

BACKGROUND OF THE INVENTION

Semiconductor integrated circuits with a plurality of semiconductor layers are fabricated by deposition, photolithography, etching, implantation, and thermal processes, repeatedly. In photolithography, overlap accuracy of patterns transferred on semiconductor layers is critical for semiconductor device fabrication.

FIG. 1A shows a top view of a wafer 1 which is divided into several zones by scribe lines. A plurality of checking patterns are exposed inside predetermined zones 50. The checking patterns are arranged vertically to each other to measure the overlap error between the patterns on adjacent semiconductor layers in two dimensions. When the checking patterns on separate semiconductor layers overlap accurately, the resulting target patterns 60 align with each other accurately. FIG. 1B shows checking patterns formed by conventional photomask exposing. In FIG. 1B, a rectangular checking pattern 12 is formed on a first semiconductor layer 10 and a square checking pattern 22 is formed on a second semiconductor layer 20, wherein the rectangular checking pattern 12 lies at the center of the square checking pattern 22 and the four sides of the rectangular checking pattern 12 are parallel to the four sides of the square checking pattern

22 correspondingly. When the rectangular checking pattern 12 is located at the center of the square checking pattern 22, the target patterns on the other zones of the first semiconductor layer 10 are accurately overlapped with the target patterns on the other zones of the second semiconductor layer 20. Furthermore, as shown in FIG. 1B, a rectangular checking pattern 12 is formed on a first semiconductor layer 10 and a square checking pattern 32 is formed on a third semiconductor layer 30, wherein the rectangular checking pattern 12 lies at the center of the square checking pattern 32 and the four sides of the rectangular checking pattern 12 are parallel to the four sides of the square checking pattern 32 correspondingly. When the rectangular checking pattern 12 is located at the center of the square checking pattern 32, target patterns on the other zones of the first semiconductor layer 10 are accurately overlapped with target patterns on the other zones of the third semiconductor layer 30.

Moreover, as shown in FIG. 1B, two rectangular checking patterns 42A and 42B are formed in a fourth semiconductor layer 40, wherein the rectangular checking pattern 42A is parallel to the rectangular checking pattern 12 in the Y-axis and the rectangular checking pattern 42B is parallel to the rectangular checking pattern 22 in the X-axis.

The disadvantage of conventional alignment of checking patterns is that target patterns on the third and fourth semiconductor layers 30 and 40 frequently misalign in the X-axis. Generally, the square checking pattern 32 on the third semiconductor layer 30 is assumed to be aligned with the square checking pattern 22 on the second semiconductor layer 20 along the X-axis, and therefore, when the rectangular checking pattern 42b on the fourth semiconductor layer 40 is

aligned with the square checking pattern 22 on the second semiconductor layer 20 in the X-axis, the target patterns on the fourth semiconductor layer 40 should be aligned with the target patterns on the third semiconductor layer 30 along the X-axis. However, the square checking pattern 32 on the third semiconductor layer 30 may not align precisely with the square checking pattern 22 on the second semiconductor layer 20 along the X-axis, and the resulting target patterns on the fourth semiconductor layer 40 misalign with the target patterns on the third semiconductor layer 30 along the X-axis.

SUMMARY OF THE INVENTION

To solve the disadvantage mentioned above, a method of checking overlap accuracy of patterns on four stacked semiconductor layers is provided according to the present invention. The target patterns on the fourth semiconductor layer formed by the method align with the target patterns on the first semiconductor layer along a first dimension, and the target patterns on the fourth semiconductor layer also align with the target patterns on the second and third semiconductor layer along a direction perpendicular to the first dimension.

One object of the present invention is to provide a method of checking overlap accuracy of patterns on a fourth semiconductor layer. The method comprises the following steps: forming a first checking pattern on a first semiconductor layer, a second checking pattern on a second semiconductor layer, a third checking pattern on a third semiconductor layer and a fourth checking pattern on a fourth semiconductor layer, wherein the first, second and third checking patterns overlap to form a first rectangular frame, the fourth checking pattern is surrounded by the first

rectangular frame, a first pair of parallel sides of the first rectangular frame is formed by the first checking pattern, and a second pair of parallel sides of the first rectangular frame is formed by the second and third checking patterns; measuring overlap accuracy between the fourth checking pattern and the first checking pattern; and measuring overlap accuracy between the fourth checking pattern and the second and third checking patterns

One feature of the present invention is the formation of the first checking pattern on a first semiconductor layer, the second checking pattern on a second semiconductor layer, the third checking pattern on a third semiconductor layer and a second rectangular frame as the fourth checking pattern on a fourth semiconductor layer, wherein the first, second and third checking patterns overlap to form the first rectangular frame, the fourth checking pattern is surrounded by the first rectangular frame, and the second checking pattern is parallel to the third checking pattern.

Another feature of the present invention is that two pairs of first parallel line-shaped patterns are formed on the first semiconductor layer, a pair of second parallel line-shaped patterns is formed on the second semiconductor layer, a pair of third parallel line-shaped patterns is formed on the third semiconductor layer, and a second rectangular frame as the fourth line-shaped patterns is formed on the fourth semiconductor layer. Accordingly, the first, second and third checking patterns overlap to form the first rectangular frame and the fourth checking pattern is surrounded by the first rectangular frame.

The advantages of the present invention are that the resulting target patterns on the fourth semiconductor layer align with the resulting target patterns on the first

semiconductor layer along a first dimension and the resulting target patterns on the four stacked semiconductor layers align with the resulting target patterns on the second and third semiconductor layers along a direction perpendicular to the first dimension.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given herein below and the accompanying drawings, given by way of illustration only and thus not intended to be limitative of the present invention. In the drawings,

FIG. 1A is the top view of a wafer showing a plurality of checking patterns formed inside the scribe lines;

FIG. 1B illustrates the checking patterns formed by conventional aligner photomask;

FIG. 2A shows a first checking pattern formed on a first semiconductor layer according to the first embodiment in the present invention;

FIG. 2B shows a second checking pattern formed on a second semiconductor layer according to the first embodiment in the present invention;

FIG. 2C shows a third checking pattern formed on a third semiconductor layer according to the first embodiment in the present invention;

FIG. 2D shows a fourth checking pattern formed on a fourth semiconductor layer according to the first embodiment in the present invention;

FIG. 3A shows a first checking pattern formed on a first semiconductor layer according to the second embodiment in the present invention;

FIG. 3B shows a second checking pattern formed on a second semiconductor layer according to the second embodiment in the present invention;

FIG. 3C shows a third checking pattern formed on a third semiconductor layer according to the second embodiment in the present invention;

FIG. 3D shows a fourth checking pattern formed on a fourth semiconductor layer according to the second embodiment in the present invention;

FIG. 4A shows one modification of the first embodiment in the present invention;

FIG. 4B shows another modification of the first embodiment in the present invention;

FIG. 4C shows still another modification of the first embodiment in the present invention; and

FIG. 4D shows one modification of the second embodiment in the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[First embodiment]

FIG. 2A shows a first checking pattern formed on a first semiconductor layer according to the first embodiment in the present invention. In FIG. 2A, the first checking pattern 110 comprises two pairs of first line-shaped patterns 110a and 110b parallel to each other and both the first line-shaped patterns 110a and 110b comprise two parallel lines. The first checking pattern 110 is formed by exposing a first photomask on the first semiconductor layer 100 and then developing the pattern 110 thereon.

FIG. 2B shows a second checking pattern formed on a second semiconductor layer according to the first embodiment in the present invention. In FIG. 2B, the second checking pattern comprises a pair of second parallel line-shaped

patterns 220. Two lines of the second parallel line-shaped patterns 220 are parallel to each other. The second checking pattern 220 is formed by exposing a second photomask on the second semiconductor layer 200 and then developing the pattern 220 thereon.

FIG. 2C shows a third checking pattern formed on a third semiconductor layer according to the first embodiment in the present invention. In FIG. 2C, the third checking pattern comprises a pair of third parallel line-shaped patterns 330. Two lines of the third parallel line-shaped patterns 330 are parallel to each other. The third checking pattern 330 is formed by exposing a third photomask on the third semiconductor layer 300 and then developing the pattern 330 thereon.

As FIG. 2C shows, the two pairs of first line-shaped patterns 110a and 110b, the pair of second parallel line-shaped patterns 220 and the pair of third parallel line-shaped patterns 330 are arranged to form a first rectangular frame 500. The first pair of parallel sides 510 of the first rectangular frame 500 is constructed by the first line-shaped patterns 110a and 110b, and the second pair of parallel sides 520 of the first rectangular frame 500 is constructed by the second parallel line-shaped patterns 220 and the third parallel line-shaped patterns 330. The third parallel line-shaped patterns 330 are located outside the second pair of parallel sides 520 of the first rectangular frame 500 and the second parallel line-shaped patterns 220 are located inside the second pair of parallel sides 520. Accordingly, the interval between the two lines of the third parallel line-shaped patterns 330 is larger than the interval between the two lines of the second parallel line-shaped patterns 220.

FIG. 2D shows a fourth checking pattern formed on a fourth semiconductor layer according to the first embodiment in the present invention. The fourth checking pattern 440 is formed by exposing the fourth photomask on the fourth semiconductor layer 400 and then developing the pattern 440 thereon. As FIG. 2D shows, the fourth photomask defines a second rectangular frame 600 as the fourth checking pattern 440 constructed by four lines on the fourth semiconductor layer 400 and the fourth checking pattern 440 is surrounded by the first rectangular frame 500.

After the checking patterns are formed on the four stacked semiconductor layers, overlap accuracy of the resulting target patterns on the four semiconductor layer is measured by overlay scanning. As FIG. 2D shows, the center position Y0 of the first checking pattern 110 along the first dimension (i.e. Y-axis) is obtained and the center position Y1 of the fourth checking pattern 440 along the Y-axis is also measured. When the difference between Y0 and Y1 is within a predetermined error range, the resulting target patterns on the fourth semiconductor layer align with those on the first semiconductor layer along the Y-axis.

Subsequently, the center positions of the second checking pattern and the third checking pattern are measured by overlap scanning. A first average position X01 along the second dimension (i.e. X-axis) between the second checking pattern 220 and the third checking pattern 330 on one side is measured. A second average position X02 between the second checking pattern 220 and the third checking pattern 330 on the other side is then measured. An average value of the first average position X01 and the second average position X02 is obtained to represent the center position X0 of the second checking pattern 220 and the third checking pattern

330. Subsequently, the center position X1 of the fourth checking pattern 440 along the X-axis is measured. When the difference between X0 and X1 is within a predetermined error range, the resulting target patterns on the fourth semiconductor layer align with those on the second and third semiconductor layers along the X-axis.

[Second Embodiment]

FIG. 3A shows a first checking pattern formed on a first semiconductor layer according to the second embodiment in the present invention. In FIG. 3A, the first checking pattern comprises a pair of first parallel line-shaped patterns with two parallel lines. The first checking pattern 110 is formed by exposing a first photomask on the first semiconductor layer 100 and then developing the pattern 110 thereon.

FIG. 3B shows a second checking pattern formed on a second semiconductor layer according to the second embodiment in the present invention. In FIG. 3B, the second checking pattern comprises the second line-shaped pattern 220 located on one side of the first checking pattern 110 and perpendicular to the first checking pattern 110. The second checking pattern 220 is formed by exposing a second photomask on the second semiconductor layer 200 and then developing the pattern 220 thereon.

FIG. 3C shows a third checking pattern formed on a third semiconductor layer according to the second embodiment in the present invention. In FIG. 3C, the third checking pattern comprises the third line-shaped pattern 330 located on one side of the first checking pattern 110 and perpendicular to the first checking pattern 110. The third checking pattern 330 is formed by exposing a third photomask on the third semiconductor layer 300 and then developing the pattern 330 thereon.

As FIG. 3C shows, the pair of first parallel line-shaped patterns 110, the second line-shaped pattern 220 and the third line-shaped pattern 330 are arranged to form a first rectangular frame 500. The first pair of parallel sides 510 of the first rectangular frame 500 is constructed by the first parallel line-shaped patterns 110, and the second pair of parallel sides 520 of the first rectangular frame 500 is constructed by the second line-shaped pattern 220 and the third line-shaped pattern 330. The third line-shaped pattern 330 is parallel to the second line-shaped pattern 220 and the second and third line-shaped patterns are on the two sides of the second pair of parallel sides 520 of the first rectangular frame 500 respectively.

FIG. 3D shows a fourth checking pattern formed on a fourth semiconductor layer according to the second embodiment in the present invention. The fourth checking pattern 440 is formed by exposing the fourth photomask on the fourth semiconductor layer 400 and then developing the pattern 440 thereon. As FIG. 3D shows, the fourth photomask defines a second rectangular frame 600 as the fourth checking pattern 440 constructed by four lines on the fourth semiconductor layer 400 and the fourth checking pattern 440 is surrounded by the first rectangular frame 500.

After the checking patterns are formed on the four stacked semiconductor layers, overlap accuracy of the resulting target patterns on the four semiconductor layer is measured by overlay scanning. As FIG. 3D shows, the center position Y'0 of the first checking pattern 110 along the first dimension (i.e. Y-axis) is obtained and the center position Y'1 of the fourth checking pattern 440 on the fourth semiconductor layer along the Y-axis is also measured. When the difference between Y'0 and Y'1 is within a predetermined

error range, the resulting target patterns on the fourth semiconductor layer align with those on the first semiconductor layer along the Y-axis.

Subsequently, the center positions of the second checking pattern and the third checking pattern are measured by overlap scanning. The position X'01 of the second checking pattern 220 on one side of the second pair of parallel sides 520 and the position X'02 of the third checking pattern 330 on the other side of the second pair of parallel sides 520 are measured. A average value of the position X'01 and the position X'02 is obtained to represent the center position X'0 of the second checking pattern 220 and the third checking pattern 330. Subsequently, the center position X'1 of the fourth checking pattern 440 along the X-axis is measured. When the difference between X'0 and X'1 is within a predetermined error range, the resulting target patterns on the fourth semiconductor layer align with those on the second and third semiconductor layers along the X-axis.

FIG. 4A shows one modification of the first embodiment in the present invention. The third parallel line-shaped patterns 330 are located inside the second pair of parallel sides 520 of the first rectangular frame 500 and the second parallel line-shaped patterns 220 are located outside the second pair of parallel sides 520. Accordingly, the interval between the two lines of the second parallel line-shaped patterns 220 is larger than the interval between the two lines of the third parallel line-shaped patterns 330. The third parallel line-shaped patterns 330 are parallel to the second parallel line-shaped patterns 220.

FIG. 4B shows another modification of the first embodiment in the present invention. The fourth checking pattern 440 is formed by exposing the fourth photomask on the

fourth semiconductor layer 400 and then developing the pattern 440 thereon. As FIG. 4B shows, the fourth photomask defines a second rectangular pattern as the fourth checking pattern 440 on the fourth semiconductor layer 400 and the fourth checking pattern 440 is surrounded by the first rectangular frame 500.

FIG. 4C shows still another modification of the first embodiment in the present invention. The fourth checking pattern 440 is formed by exposing the fourth photomask on the fourth semiconductor layer 400 and then developing the pattern 440 thereon. As FIG. 4C, the fourth photomask defines a second rectangle frame 600 as the fourth checking pattern 440 on the fourth semiconductor layer 400 and the first rectangular frame 500 is surrounded by the fourth checking pattern 440.

FIG. 4D shows one modification of the second embodiment in the present invention. The fourth checking pattern 440 is formed by exposing the fourth photomask on the fourth semiconductor layer 400 and then developing the pattern 440 thereon. As FIG. 4D, the fourth photomask defines a second rectangular frame 600 as the fourth checking pattern 440 on the fourth semiconductor layer 400 and the first rectangular frame 500 is surrounded by the fourth checking pattern 440.

If the difference between X0 and X1 and /or the difference between Y0 and Y1 are not within the corresponding predetermined error ranges, which means the target patterns on the fourth semiconductor layer misalign with those on the first, second and/or third semiconductor layers, the patterns on the fourth semiconductor layer are removed and then re-exposed to form aligned patterns.

The overlap accuracy of the target patterns on four stacked semiconductor layers is checked according to the

first and second embodiments in the present invention. The overlap accuracy of the target patterns on the first and the fourth semiconductor layer is measured along the first dimension and the overlap accuracy of the target patterns on the second, third and fourth semiconductor layer is measured along a direction perpendicular to the first dimension.

The foregoing description of the preferred embodiments of this invention has been presented for purposes of illustration and description. Obvious modifications or variations are possible in light of the above teaching. The embodiments were chosen and described to provide the best illustration of the principles of this invention and its practical application to thereby enable those skilled in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the present invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.